An Inexpensive Megabit Packet Radio System

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ABSTRACT

Although packet radio is relatively new to the amateur radio community, there are now over 10,000 amateur packet radio units in service. These units cost between $500 and $800, including the controller and radio, and generally operate at 1200 baud. An effort to improve performance significantly while keeping costs reasonable has resulted in a packet radio system that can operate at data rates of up to one megabit per second, yet costs less than $1,000 for the controller and radio. The controller is based on an IBM-PC-equivalent processor board, which simultaneously controls the radio and interfaces directly to terminals, host computers, or a local area network. The controller can also be used to develop its own software. The radio is digitally synthesized and operates in the 400 MHz to 500 MHz region. The system uses DoD Internet IP/TCP datagrams, and has been used in the amateur radio service at the maximum legal data rate of 56 Kbps.

1. INTRODUCTION

This paper describes a low-cost megabit packet radio system designed and built by members of the Amateur Radio Group, WB6MXZ, at the University of Southern California's Information Sciences Institute (ISI). The protocols, data rates, and modulation techniques used in this system are similar to those used in cable-based local area networks.

We began this effort after experimenting with off-the-shelf packet radio equipment. Our experience with that equipment showed that 1200 baud was too slow to be very useful. A review of local area network technology showed us that high data rates could be supported by simple, low-cost equipment. As a result, we decided to design and build a megabit packet system costing under $1,000.

The following sections describe the motivation for the work, the design objectives, the system hardware and protocol, and the experimental results. Conclusions drawn from the project are also presented.

2. BACKGROUND

The megabit radio system was the outgrowth of earlier amateur packet radio work by the ISI group, in which we first demonstrated land and aeronautical mobile amateur packet radio operation, as well as transcontinental and intercontinental internetwork communications using amateur packet radio [6] [7] [8] [9].

Our early packet radio work used first-generation, 1200 baud amateur packet radio boards (commonly referred to as "Vancouver boards"). For the experiments, one of the packet radios was outfitted as a self-contained mobile unit that could be used in a car, boat, or airplane. The mobile unit consisted of the Vancouver board itself, an ASCII terminal, a small monitor, and a handheld two-meter radio transceiver, all battery powered. The Vancouver board and its software were modified to support internetworking to any host on the ARPANET [2] via connection to a mainframe computer at ISI.

In March 1982, we demonstrated mobile, transcontinental internetworking using amateur packet radio. The mobile packet radio unit was driven in a van around the Los Angeles basin, and then flown above the area in a Cessna-T210. The mobile unit was in contact with a packet station at ISI, and was linked via the ARPANET to a terminal in Virginia. An interactive transcontinental digital conversation was conducted while the van traveled the LA freeway system, and continued while the plane flew over Los Angeles and the Santa Monica Bay.

Later that same year, the authors established an intercontinental internetwork link between The Hague, Netherlands and Los Angeles using seven different networks including the ARPANET, the DARPA Packet Satellite Network and INTELSAT IVa, and our low-speed amateur packet radio network.

3. OBSERVATIONS ON LOW-SPEED PACKET RADIO

Although these experiments were interesting, many deficiencies in the low-speed packet system and its supporting protocol became apparent, and eventually led to the effort described in the remainder of this paper. We came to the following conclusions about existing low-speed packet radio systems:

- As shown in Table 3-1, 1200 bits per second is far too slow to support serious computer-to-human or computer-to-computer communications. After accounting for overhead, half-duplex communications, interference, and collisions, a 1200-bit-per-second channel provides less than 300 bits per second of actual data transmission capability, adequate for traffic between touch typists, but far too slow to accomplish much else.
- Typical packet controllers are too limited in hardware capability to support any but the simplest protocols, even at low speeds, or to be used for software development. These hardware limitations have inhibited protocol experimentation and development,

which might otherwise itself generate a desire for higher data rates and more robust protocols. This may have already resulted in the premature stagnation of amateur packet radio development.

- The single most insidious event in amateur packet radio development was the adoption of the Intel 8273 HDLC/SDLC Protocol Controller chip as a packet radio protocol standard. Because of this, "Synchronous NRZI HDLC" became synonymous with "amateur packet radio." Although the Intel chip had the beneficial effect of forcing a standardization of a packet frame, its contents, and the bit encoding, it had the sinister effect of precluding the use of countless home computers (including Apples, Ataris, Commodores, TIs, and Timex/Sinclairs) as packet controllers, and of unduly increasing packet controller cost. Many amateurs have lost sight of the fact that synchronous, NRZI HDLC frames are not needed for packet communications at 9600 bits per second or less. Packetized asynchronous serial bit streams work perfectly well. Unfortunately, much of the pioneering work done by Harold Price (NK6K), Dave Henderson (KD4NL), and some Canadian amateurs in the field of asynchronous packets has fallen on deaf ears.
- Packet controllers are far too expensive for the limited capability they provide. Part of the expense is caused by the requirement to support HDLC. However, most of the problem results from amateurs who build everything from scratch instead of adapting available computing hardware for use as a packet controller. (There has been one notable exception, the adaptation of the Xerox 820 processor board for use as a packet controller [1].)

Table 3-1: Why 1200 bits per second is too slow

```
With a 150-character packet,

   1200 bits per second
 -       packet overhead
 -       carrier sense backoff time
 -       transmitter keying time
   ====
    600 bits per second
 -       half duplex
   ====
    300 bits per second
 -       channel interference/errors
 -       collisions with other users
   ====
  < 300 bits per second ... Typing Speed!
```

4. HIGH-SPEED PACKET RADIO PROJECT

The low performance of amateur equipment contrasts sharply with that of existing commercial and military equipment. For example, local area network controllers and interfaces operate at megabit data rates, using proven technology, for a few thousand dollars per node. Thus it seemed possible for us to build a packet radio system with vastly improved performance for little extra cost, and we began a project to do exactly that.

The primary goals of the project were as follows:

- Cost: The system should cost less than $1,000, including both the radio and the controller.
- Data rate: The system should operate at up to one megabit per second (FCC regulations limited over-the-air tests to 56 Kbps in the amateur bands).
- Controller: The controller should be a microprocessor with an address space well in excess of 64K. (We later realized that the controller should be based on some widely available microcomputer and should also provide its own software development environment.)
- Protocols: The protocols should match those of an internetwork environment, such as the DoD's ARPANET.
- Frequency: The radio should digitally synthesized and usable in the 400-500 MHz spectrum.
- Bandwidth: The system should be usable in a 6 MHz television channel or equivalent.

In summary, our major objective was to build a packet radio system providing at least 500 times the performance of existing systems at no more than twice the cost.

5. HARDWARE

5.1. Hardware Overview

The system hardware (Figure 5-1) is composed of a Packet Controller, and a radio (a digitally controlled transmitter and receiver), with commercially available modules being used wherever possible. The Packet Controller was designed around an IBM-PC-equivalent mother board, with the addition of a custom serial controller board to support the high-speed data path to the radio. The radio was designed around a commercial downconverter and power amplifier module, with the remaining hardware custom designed.

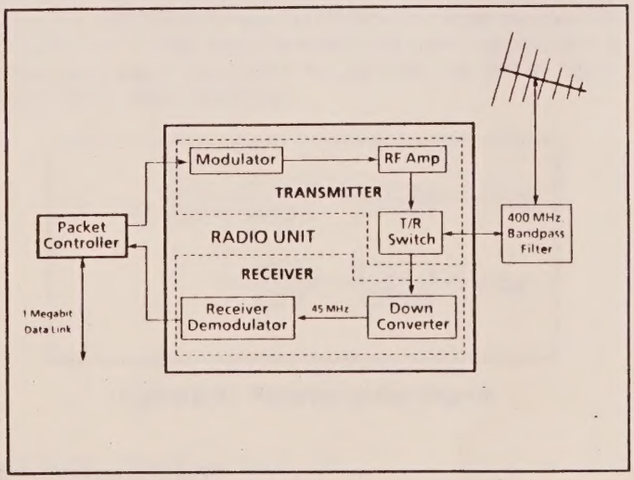


Figure 5-1: System hardware

5.2. Packet Controller

A block diagram of the controller is shown in Figure 5-2. A Faraday Model 64 IBM-PC-equivalent mother board was used for the controller. The Faraday board provided the program memory, processor, bus environment, DMA control, timers, parallel port, and low-speed serial ports required for the implementation. Local area network communications were supported by plugging an Ethernet controller board into the Faraday board. We designed an additional serial controller board to provide the required high-speed serial port, two 8-bit parallel bidirectional ports, additional EPROM space, and battery-backed-up RAM.

We chose a Zilog 8530A chip for the high-speed serial link to the radio, because it was relatively easy to interface to the IBM-PC bus and because it supported a data rate of up to one megabit. The Zilog 8530A had the additional benefit of containing an internal PLL capable of encoding and decoding data at up to 250 Kbps, the fastest of the serial chips considered. (For data rates in excess of 250 Kbps an external PLL is required.)

In addition to providing the high-speed serial link to the radio, the 8530A chip also provided the capability for high-speed serial communication to the host computer. An 8-bit bidirectional port provided optional high-speed host support, while lower speed hosts and terminals were connected via standard RS-232 connections.

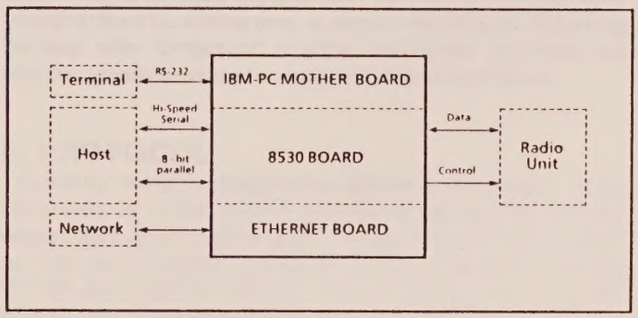


Figure 5-2: Controller diagram

5.3. Transmitter

A block diagram of the transmitter is shown in Figure 5-3. It consists of a digital PLL (to control transmit frequency), a frequency shift keying (FSK) modulator, an RF preamp and 10-watt amplifier, a solid-state T/R switch, and transmit control logic (to power down the RF preamp and amplifier, and control the T/R switch).

The transmitter uses a digital PLL for center frequency synthesis, derived from a 16 MHz crystal reference. The PLL employs a dual-modulus prescale control section and a second-order low-pass filter to derive the loop error voltage. The loop center frequency is controlled by rotary switches that select the value of the loop divisor. (For frequency-agile applications, the switches can be replaced with a computer interface.) The reference oscillator is divided down by the M divider to 100 KHz, which is the basic loop control frequency and one-fifth the synthesizer's minimum step size.

The control voltage derived from the PLL is fed to the VTO, which directly generates the 400 MHz carrier frequency. The transmit center frequency is controlled by the PLL, but the digital data input to a VTO bias switch causes the frequency to shift at the data rate, thus generating the FSK output. The oscillator output is split by a hybrid divider to feed the RF preamp stages and feed back to the prescale divide loop. The RF preamp section feeds a 10-watt final amplifier stage that couples to the antenna through the solid-state T/R switch.

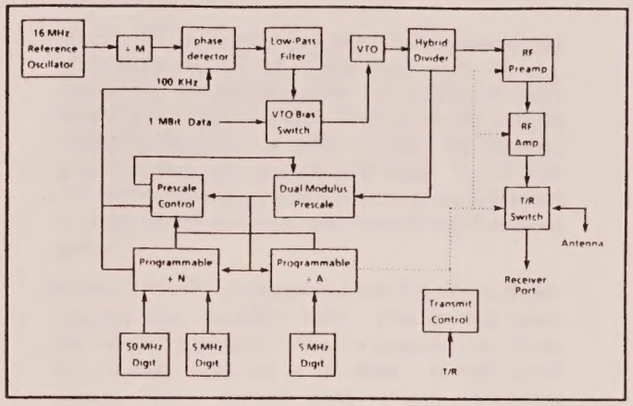


Figure 5-3: Transmitter diagram

The T/R switch was implemented with PIN diodes and quarter-wavelength stubs inside the transmitter. The PIN diode bias voltage is controlled by FETs to provide very fast response and good isolation between transmitter and receiver.

A sixth-order elliptical bandpass interdigital filter was used between the radio and the antenna to suppress spurious emissions. The external filter provided frequency selectivity for both the receiver and the transmitter.

5.4. Receiver

Figure 5-4 is a block diagram of the receiver section. It consists of a commercial downconverter (to convert the 400 MHz RF to the 45 MHz IF frequency), a commercial FM receiver circuit with IF amplifiers and a tunable discriminator (to demodulate the data stream), a differential comparator (to recover the baseband data), a tuned log amplifier strip (to detect the carrier signal), and a hysteresis voltage comparator (to generate the carrier detect signal for the packet controller).

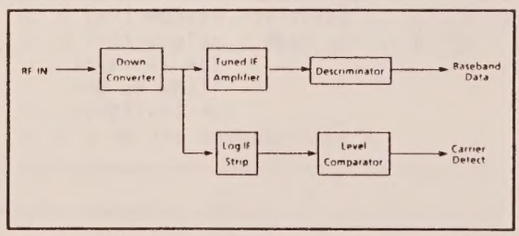
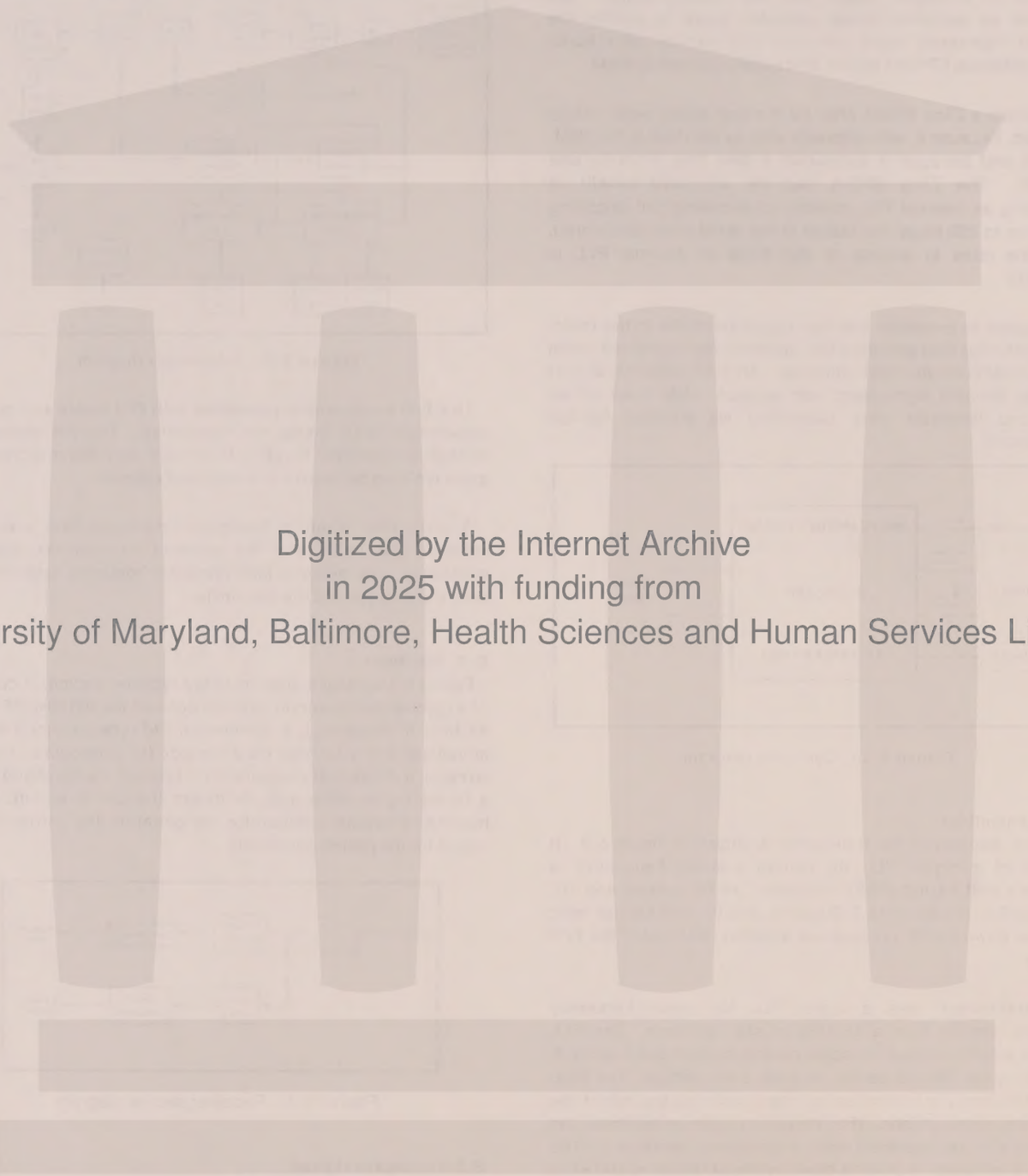


Figure 5-4: Receiver section diagram

5.5. Hardware Issues

Several of our important hardware decisions were influenced by cost considerations. For example, we chose FSK because it was simpler and less expensive than phase encoded approaches. Normally, a PLL capable of controlling the two frequencies of an FSK transmission would have to relock in a fraction of a bit time



to properly control both the "one" and "zero" frequencies. Loop relock time required to support a one-megabit data rate would be about 100 nanoseconds. A PLL capable of this performance would be complex and costly.

To support the choice of FSK modulation and to avoid a costly PLL, we chose Bi-Phase Space Modulation (FM0) for the base-band modulation scheme. FM0 encoding relaxes the required loop performance by inserting half-width pulses in the data stream to maintain a "zero-mean" signal, i.e., FM0 encoding guarantees that the data stream spends equal time in "zero" and "one" states, independent of the actual data transmitted. This results in a constant mean output frequency for the loop to lock onto. The lower performance loop, required for FM0, locks to the arithmetic mean of the two FSK frequencies over a period of several thousand data bits to provide stable frequency control at reduced cost. The radio equipment must, however, support a bandwidth of twice the unencoded data rate. For example, a one-megabit data rate requires the radio to support pulse durations of 500 nanoseconds.

Receiver sensitivity was found to be limited by in-band energy generated by the transmitter's PLL. To increase the receiver sensitivity, the transmit control logic was designed to change the PLL divider value, which pulls the VTO frequency out-of-band during receive. While the channel turnaround response time of the transmit modulator, RF section, and receive-carrier detect is about 5 microseconds, the practical radio link turnaround time, limited by the PLL settling time, is about 1 millisecond. Relocking the loop after turnaround restricts the system dynamics, but provides greatly increased sensitivity in the receive circuit.

6. PROTOCOL

Currently, there is considerable debate in the amateur radio community as to the network protocol to be used for amateur packet radio communications [3]. Virtual Circuit protocols, such as X.25, and datagram protocols, such as the DoD's Internet IP/TCP, are major contenders. For our packet work, we chose Internet IP/TCP datagrams for the following reasons:

- Internet IP/TCP datagrams enabled us to connect the packet radio network to other networks. Our prior packet radio work convinced us that network interconnectivity was key to the success of any high-speed network.
- Datagrams provide more flexibility in packet routing than virtual circuit switching. In a virtual circuit protocol network, routes are fixed at connection time, while in a datagram protocol network, packet routes are determined on a per-packet basis. Thus, datagrams can be routed dynamically, to account for station movement or changes in the transmission path. In a radio environment, this capability provides a distinct advantage over virtual circuits, where the entire circuit must be destroyed and reestablished for each route change.
- Datagrams permit a wider choice of modes and services. A major reason for building a high-speed packet network is to allow the use of modes and services not possible on slower networks. Examples include real-time packet speech and video. Virtual circuit protocols, designed exclusively for reliable transmission, are poor candidates for these and other services, for which the timeliness of data delivery is more important than the accuracy of the data. The key is that applications requiring "speed" can employ IP without TCP, while those requiring "robustness" can employ both TCP and IP; with X.25, there is no option but to accept the reliability mechanisms.
- Internet IP/TCP datagrams allow the immediate use of a large number of higher-level protocols and services by our packet radios. The Internet IP/TCP-based protocol suite contains protocols for terminal character streams as well as mail, file transfer, graphics, facsimile, speech, and video. Use of X.25 virtual circuits would have forced us to implement not only the packet software, but many of these services as well.
- Internet IP/TCP datagrams allow the use of larger packets than standard X.25. This permits fewer packets to be used to transmit a given number of bits on channels with low error rates. In high-speed packet radio environments, where transmitter turnaround time and other per packet costs dominate, this represents a significant savings. (Also, in such an environment, header size differences between between IP/TCP and X.25 are insignificant.)

7. EXPERIMENTAL RESULTS

The megabit packet radio system was designed, built, and tested in 1983 [4], and exhibited at the 1983 ARRL Southwest Convention [5]. Tables 7-1 and 7-2 summarize controller and radio features. Figures 7-2 and 7-3 show the controller and the radio, respectively.

Table 7-1: Packet Controller Features

- o 8088-based, with software written in C and assembly language
- o Up to 40K EPROM, 256K DRAM, 2K CMOS battery backed-up SRAM
- o 3 x 8 bit parallel I/O ports
- o 4 channel DMA capability
- o 2 full-duplex low-speed serial ports
- o 2 full-duplex 1 Mbps serial ports
  - Internal PLL
  - FM0 or NRZI
  - RS-232/RS-422
- o 3 x 16 bit counter/timers

Table 7-2: Radio Features

- o 10 watts RMS on UHF
- o Synthesized crystal-controlled PLL
- o Direct FSK carrier modulation
- o Data rates to 1 Mbps
- o 6 pole elliptical band-pass interdigital filter

Packet radios were deployed in the Los Angeles area for operational testing in November 1983. The tests were conducted in the 400 MHz Amateur Radio band, between stations five miles apart. No line-of-sight path was available between the stations; signals had to be bounced off a nearby building. During the tests, the radio link was operated at 56 Kbps (the maximum allowed data rate in that band) to provide a high-speed, error-free connection between a remote user's personal computer and a large time-sharing central system.

While the field test proved the feasibility of high-speed packet communication, the limits of radio performance were determined in the laboratory. An experimental test setup was established, as shown in Figure 7-1, to simulate high-speed data traffic and to verify performance. The packet radios were operated at the full one-megabit rate with a simulated path loss of 120 dB, corresponding to an expected radio range of 25 miles at 400 MHz. The turnaround time was measured by alternately pulsing the T/R control lines of the two radios and measuring the time required for first data recovery.

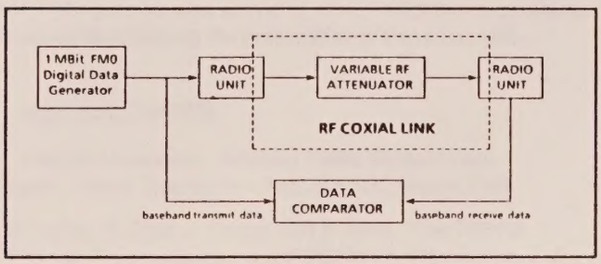


Figure 7-1: Experimental test setup

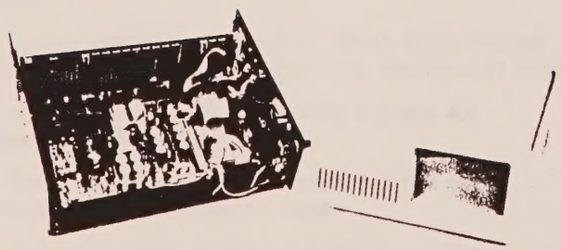


Figure 7-2: Packet controller

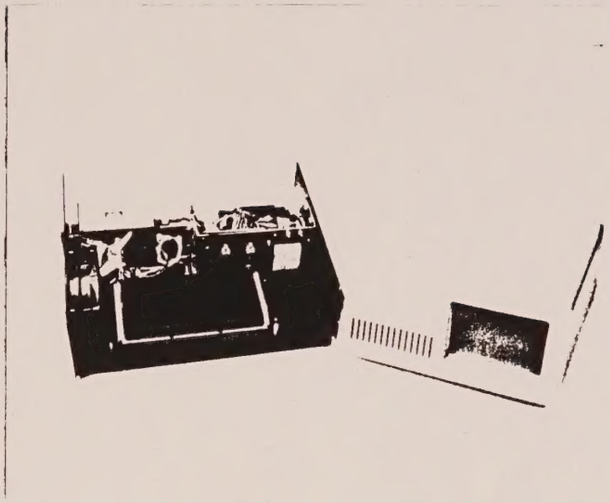


Figure 7-3: Radio

8. CONCLUSIONS

Use of DoD Internet IP/TCP datagrams for the packet protocol had positive results. It allowed us to connect our network to other networks, and to experiment with a wide variety of higher-level protocols and services, such as computer mail and file transfers. By using datagrams, our experiments were not restricted to low-level, point-to-point terminal linking.

Our decision to use a commercial IBM-PC-equivalent mother board for the controller, instead of following the more traditional "NIH/RYO" (Not Invented Here, Roll Your Own) mentality, played a key role in the success of the project. It allowed us to immediately begin developing hardware and software on existing PCs. It permitted our hardware and software development and testing to be carried out in a common, tool-rich development environment that included editors, compilers, assemblers, linkers, and debuggers. It also allowed us to use externally developed hardware and software, such as the Ethernet boards, to connect to local area networks.

The increased popularity of the IBM-PC has, in retrospect, made our decision look even better. In the summer of 1983, PC-compatible mother boards were selling for $495, quantity 1. By the summer of 1985, the price had dropped to $135, quantity 1. At this latter price, a megabit PC-based packet controller could be assembled for about the same price as current commercial 1200 baud units.

As a beneficial side effect, packet controllers can even be used outside the radio environment. Our packet controllers have been used, without the radio, as a "network extension cord" to provide computer access to a new block of offices at ISI. Their small size and ease of deployment facilitate their use for temporary high-speed communications.

In summary, by using the synergism of commercially developed hardware and available network protocols and software, a robust, high-speed packet radio system can be built for little more than today's low-speed systems. Such a system not only provides the high-level protocols, services, and performance lacking in today's low-speed systems, but also provides an environment for amateurs to develop and experiment with their own unique protocols.

9. POSTSCRIPT

The favorable results of this effort have encouraged us to undertake a more ambitious effort, the development of a low-cost (under $1,000), moderate-speed (up to 200 Kbps), spread-spectrum packet radio system based on the same PC controller and a custom-designed VLSI digital correlator.

10. ACKNOWLEDGMENTS

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